

Electrothermal Modeling of Multi-Fingered PHEMTs Applying a Global Approach

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Abstract — In this paper, a global method is proposed to characterize the electrothermal behavior of multi-fingered Pseudomorphic High Electron-Mobility Transistors (PHEMTs). The method is based on the coupling of circuit, electromagnetic and thermal softwares. It is shown that scaling rules have just to be applied for intrinsic performances of a transistor when extrinsic elements and thermal effects are rigorously taken into account.

I. INTRODUCTION

To model the electrothermal behavior of microwave devices, an electrical equivalent circuit is classically used where the active, passive and thermal parts are described in lumped elements form. However, as the complexity and the high integration of circuits increase, a more accurate modeling, especially of electromagnetic (EM) interactions and self heating phenomena, becomes necessary. The global approach proposed here allows to determine these contributions in the device model applying different rigorous analysis techniques.

This approach combines circuit, electromagnetic and thermal softwares. An equivalent scheme is required in order to solely characterize the intrinsic domain of the component. The extrinsic domain is determined by an electromagnetic simulator providing a [S] matrix and the self heating effects are taken into account through a thermal impedance matrix [Z] obtained from a 3D thermal simulation. Fig. 1 illustrates the synoptic of the electrothermal simulation which is performed where Pd and Ta represent respectively the dissipated power into the transistor and the ambient temperature.

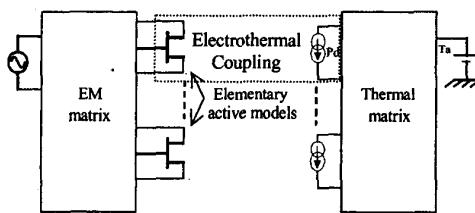


Fig. 1. Synoptic of the global electrothermal simulation.

The aim of this paper is to describe the different steps of the global approach which is proposed. This method is applied to 4x80 μm and 8x120 μm PHEMTs. The technologic particularity of this topology is that each source electrode is grounded to a plated heat sink through via holes. This substrate thinning under the transistor active region allows to reduce the thermal resistance [1].

In Section II, the linear modeling, based only on the coupling of EM and circuit softwares, is presented. The 4x80 μm PHEMT is considered as the reference component of this analysis. The accuracy of the global method is demonstrated by predicting the 8x120 μm PHEMT linear response. In this case, an electromagnetic simulation of the new passive domain is only required.

The transistor active model is deduced from the reference component results applying straightforward scaling rules. The validity of this methodology, applied to a field effect transistor small-signal global modeling, has already been proved [2].

We are then able to extend in Section III this global method to the non linear modeling. Thus, the thermal simulator is combined with the electromagnetic and circuit ones to establish the 8x120 μm PHEMT electrothermal model. First load-pull measurements have been performed at 20 GHz and show good agreements with the non linear model.

II. THE PHEMT SMALL SIGNAL MODEL

For this linear analysis, the reference component is the 4x80 μm PHEMT presented Fig. 2.

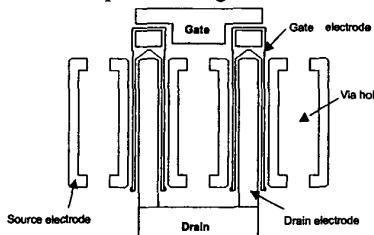


Fig. 2. Distributed passive part of the 4x80 μm PHEMT.

A. Global study of the 4x80 μm PHEMT

To model the passive part of the transistor taking into account all its metalizations, two electromagnetic softwares are used.

First, a 2.5-D simulator (Agilent Momentum) based on the Moment Method (MoM) is applied. This simulation leads to reasonably good results with a reduced calculation time. The second EM software used in this study has been developed in our laboratory. This 3-D simulator is based on the Finite Element Method (FEM) defined in the frequency domain. More accurate models are provided applying this simulation with yet a very significant computing time required for multi-fingered PHEMTs analysis.

These two EM simulations allow to establish a generalized [S] matrix which replaces the lumped extrinsic elements of an electrical model. Each meshed structure, obtained from the 2.5-D and 3-D softwares, contains several localized accesses for connecting the transistor active part to its distributed domain.

An optimization on the classical PHEMT small-signal equivalent scheme is then realized in order to isolate an intrinsic model of the real part of the transistor. This intrinsic model is valid for a defined single bias point and a defined frequency range. The intrinsic model extraction being function of the EM simulation results, two different models are characterized : one corresponding to the 2.5-D simulation and the other to the 3-D simulation.

These active parts, independent from all the EM parasite couplings, are then sliced into elementary models which are chained to the corresponding extrinsic domain thanks to localized accesses. As these accesses are distributed on each transistor electrode, four equal elementary fingers are taken into account in the 4x80 μm PHEMT study.

Comparisons between global simulations and measurements from 2 to 40 GHz show good agreements, as seen Fig. 3 and 4. These linear results are obtained for a bias $V_{\text{gs}} = -0.31$ V, $V_{\text{ds}} = 5.02$ V and $I_{\text{d}} = 12.57$ mA.

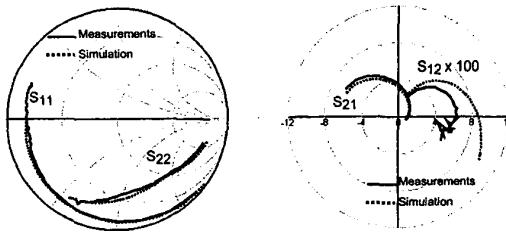


Fig. 3. 4x80 μm PHEMT linear results applying the 2.5-D simulation.

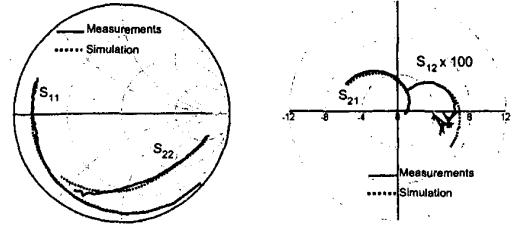


Fig. 4. 4x80 μm PHEMT linear results applying the 3-D simulation.

B. Prediction of the 8x120 μm PHEMT results

One of the main advantage of this global approach is that we can predict the response of other transistor topologies conceived with the same technology.

Thus, in order to establish the 8x120 μm PHEMT small-signal response, only EM simulations of the new distributed domain are necessary. The intrinsic models, defined in the reference transistor study, can be applied to the 8x120 μm PHEMT. Scaling rules have just to be respected when these models are sliced into elementary models. In this case, eight equal elementary fingers are taken into account. Fig. 5 and 6 prove the validity of our approach until 40 GHz, applying the 2.5-D simulation as well as the 3-D one. These prediction results are shown for a bias $V_{\text{gs}} = -0.37$ V, $V_{\text{ds}} = 5.09$ V and $I_{\text{d}} = 39.57$ mA.

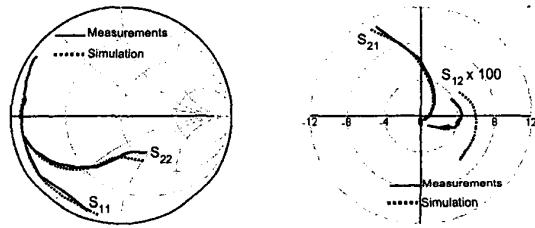


Fig. 5. Linear results of the 8x120 μm PHEMT prediction applying the 2.5-D simulation.

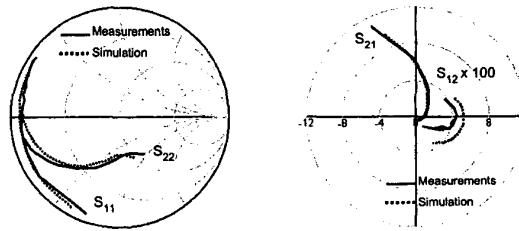


Fig. 6. Linear results of the 8x120 μm PHEMT prediction applying the 3-D simulation.

III. THE PHEMT LARGE SIGNAL MODEL

In this section, we extend our global method to the 8x120 μm PHEMT non linear modeling.

For this large-signal analysis, any additional EM simulation is necessary, the [S] matrix being the same for linear and non linear models.

To model the 8x120 μm PHEMT electrothermal behavior, we have to extract a large-signal intrinsic model function of three independent variables which are the voltages between gate and source, V_{gs} , between drain and source, V_{ds} , and the temperature T .

To achieve this aim, pulsed I(V) and S-parameters measurements have been simultaneously performed with a Chuck temperature range from 22°C to 125°C.

The intrinsic model is defined from the classical PHEMT non linear equivalent circuit [3]. The lumped elements values of this scheme are obtained by a direct extraction method, based at the same time on multi-bias S-parameters measurements and a good knowledge of extrinsic elements values [4].

As it has been considered in the small-signal study, this model is then sliced into elementary intrinsic models which are chained to the 8x120 μm PHEMT [S] matrix. Within each of the eight elementary models, self heating effects make the drain current and the diodes characteristics vary when the temperature changes.

These parameters are therefore connected to the thermal impedance matrix performed separately by a 3-D thermal simulation based on the FEM. This simulation applies in linear regime the MODULEF software which has been developed at INRIA.

We obtain thus a thermal impedance matrix $[R_{\text{th}}$] which is equivalent to a thermal resistance network and takes into account the different thermal couplings between the eight gate fingers. This thermal network is described by a matrix relation (1) where T_{ci} and P_{di} represent respectively the temperature average increase under each gate and the dissipated power on the N gate fingers.

$$\begin{bmatrix} T_{\text{c}_1} \\ \vdots \\ T_{\text{c}_N} \end{bmatrix} = [R_{\text{th}}] \cdot \begin{bmatrix} P_{\text{d}_1} \\ \vdots \\ P_{\text{d}_N} \end{bmatrix} \quad (1)$$

We can observe the slight values calculated for the matrix coupling terms (2). Such results are due to the structure particular topology. Thus, matrix terms which are considered as equal to zero represent the fact that any coupling between gate fingers appears beyond two via hole.

$$[R_{\text{th}}] = \begin{bmatrix} 217.5 & 55 & 9.5 & 5.7 & 0 & 0 & 0 & 0 \\ 55 & 217.5 & 17 & 9.5 & 0 & 0 & 0 & 0 \\ 9.5 & 17 & 217.5 & 55 & 9.5 & 5.7 & 0 & 0 \\ 5.7 & 9.5 & 55 & 217.5 & 17 & 9.5 & 0 & 0 \\ 0 & 0 & 9.5 & 17 & 217.5 & 55 & 9.5 & 5.7 \\ 0 & 0 & 5.7 & 9.5 & 55 & 217.5 & 17 & 9.5 \\ 0 & 0 & 0 & 0 & 9.5 & 17 & 217.5 & 55 \\ 0 & 0 & 0 & 0 & 5.7 & 9.5 & 55 & 217.5 \end{bmatrix} \quad (2)$$

The global electrothermal model which is thus defined has been set up in the Agilent ADS circuit software (version 1.3) in compiled model form. This model includes the EM matrix, the thermal one and five non-linearities (Tajima source I_{ds} , diodes I_{gs} and I_{gd} , capacitances C_{gs} and C_{gd}).

First, a small-signal verification is performed by comparing the large-signal model linearized around a working point with S-parameters measurements from 2 to 40 GHz.

Fig. 7 illustrates the results obtained for a bias in AB class : $V_{\text{ds}}=5.09$ V and $I_{\text{d}}=59.39$ mA.

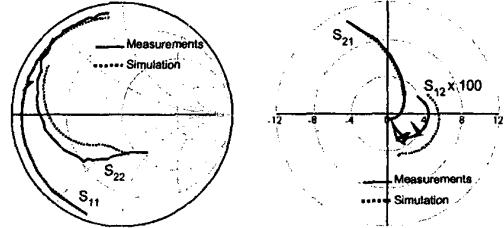


Fig. 7. Small-signal results of the 8x120 μm PHEMT non linear model.

To demonstrate the accuracy of our global method for power amplifier simulation, the compiled model has to be analyzed in large-signal regime.

The results of this non linear simulation, based on a harmonic balance method, are thus compared with load-pull measurements performed at a nominal frequency of 20 GHz for a bias $V_{\text{gs}}=0$ V, $V_{\text{ds}}=7$ V and a 50Ω load impedance.

This impedance is definitively not optimum for power performances. However, it allows us to validate the large-signal model obtained through the global approach.

A good agreement is observed between electrothermal global simulations and load-pull measurements, as seen Fig. 8 where P_{in} represents the generator available power. More measurements results will be given in the final paper.

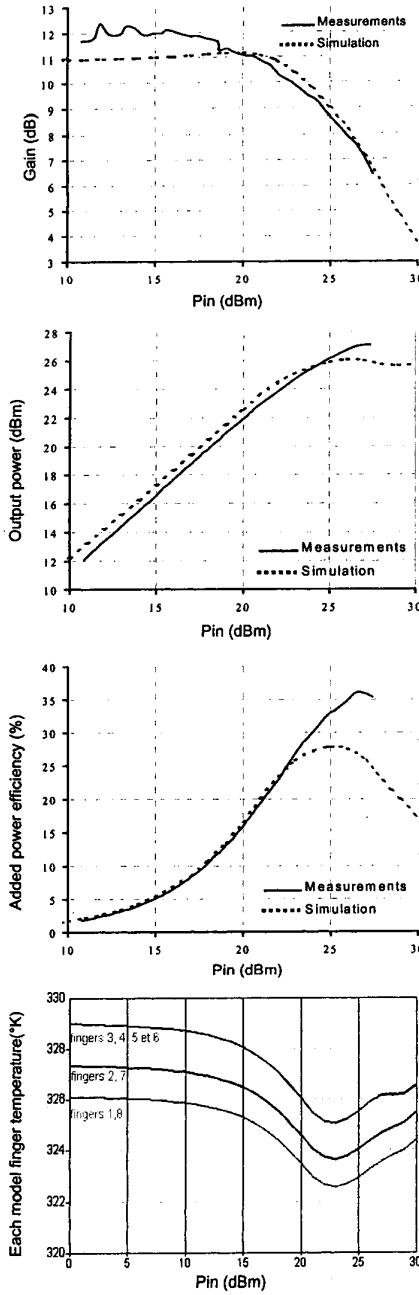


Fig. 8. Non linear results of the $8 \times 120 \mu\text{m}$ PHEMT modeling.

Besides the symmetry of the structure, this last graph underlines a slight temperature difference between all the model fingers. As it has been noticed in the introduction,

the substrate thinning under the PHEMT active part allows to reduce the thermal resistance and consequently the heating on the different component fingers.

Moreover, the added power efficiency results demonstrate a divergence beyond a generator available power of 23 dBm. That can be explained by an uncertain characterization of the average current for measurements as well as simulations.

IV. CONCLUSION

We have developed in this paper a global approach for electrothermal multi-fingered PHEMT modeling applying a circuit, an electromagnetic and a thermal software.

The methodology that has been established in this study allows to give some elementary cells combination rules to characterize very high power components.

The linear and non linear results demonstrate the accuracy of our global method to predict the response of different PHEMT topologies. This prediction requires additional electromagnetic and thermal simulations whereas straightforward scaling rules have just to be respected for the intrinsic model extraction.

This approach will be particularly useful for the design of Wide Bandgap High Power Transistors where EM and thermal couplings will be of prime importance.

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REFERENCES

- [1] T. Ishikawa, K. Okaniwa, M. Komaru, K. Kosaki, Y. Mitsui, "A high-power GaAs FET having buried plated heat sink for high-performance MMIC's", *IEEE Trans. On Electronic devices*, vol. MTT-41, pp. 3-9, 1994.
- [2] E. Larique, S. Mons, D. Baillargeat, S. Verdeyme, M. Aubourg, R. Quéré, P. Guillon, C. Zanchi, J. Sombrin, "Linear and nonlinear FET modeling applying an electromagnetic and electrical hybrid software", *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-47, pp. 915-918, June 1999.
- [3] S. Mons, E. Ducloux, E. Leclerc, L. Thibaudeau, R. Quéré, "Full electrothermal characterization of GaAs FETs", *GaAs Symp.*, pp. 123-126, 1997.
- [4] A. Laloue, J. B. David, R. Quéré, B. Mallet-Guy, E. Laporte, J. F. Villemazet, M. Soulard, "Extrapolation of a measurement-based millimeter-wave nonlinear model of PHEMT to arbitrary-shaped transistors through electromagnetic simulations", *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-47, pp. 908-914, June 1999.